Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **V1+**
2. **V2-**
3. **ALTERVATIVE V1-**
4. **INPUT**
5. **V1-**
6. **ALTERNATIVE V1+**
7. **V2+**
8. **OUTPUT**

**.081”**

**3 2 1**

**8**

**6 7**

**4**

**5**

**MASK**

**REF**

**HA-5002**

**.080”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: V- or FLOATING**

**Mask Ref: HA-5002**

**APPROVED BY: DK DIE SIZE .080” X .081” DATE: 8/25/21**

**MFG: HARRIS THICKNESS .019” P/N: HAO-5002-6**

**DG 10.1.2**

#### Rev B, 7/1